66/100 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin UNBUFFERED SO-DIMM SPECIFICATION

Revision 1.0
February 1999

Intel Corporation

Changes:

Revision 1.0 October, 1998
Added 256Mbit support, and changed decoupling.

Revision 0.7 August 14, 1998
Added clock trace length data, and PB marking information.

Revision 0.51 July 15, 1998
Added figures 14 and 15

Revision 0.5 July 14, 1998
Add support for 66MHz

Revision 0.3 June 12, 1998
Removed support of X8 components

Revision 0.22 April 15, 1998
First external copy.

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1.0 Introduction

This specification defines the electrical, mechanical, and trace routing requirements for 144-pin, 3.3 volt, 66/100 MHz, 64-bit wide (non-ECC/Parity), 2 clock, unbuffered Synchronous DRAM Small Outline Dual In-Line Memory Modules (SDRAM SO-DIMMs). These SDRAM SO-DIMMs are intended for use as main memory installed in personal notebook computer motherboards.

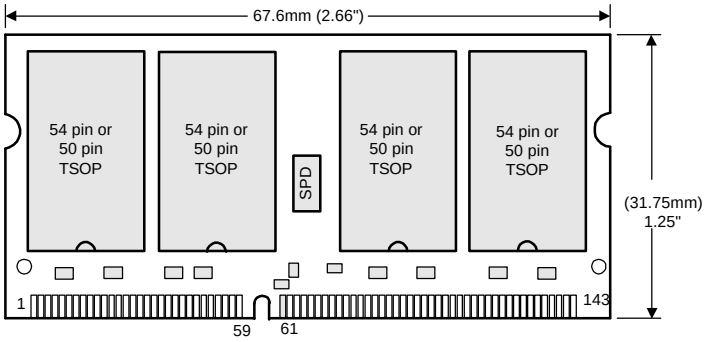


Figure 1: SO-DIMM with four 54-pin or 50-pin SDRAM per side

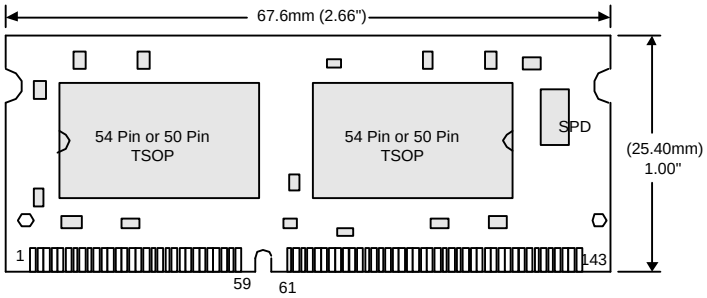


Figure 2: SO-DIMM with two 54-pin or 50-pin SDRAM per side

Related Documents

The related documents contain information that is critical to this specification. The revisions listed are the latest releases at the time of this writing. However, it is important to use the most current revisions of each of these documents when generating or modifying SO-DIMM designs.

Table 1: Related Documents

TITLE	REV	DATE
Intel PC/100 SDRAM Specification	1.62	Sept. 1998
Intel SDRAM SPD Data Structure Specification	1.2A	April 1997

SO-DIMM Configurations
SDRAM SO-DIMM configurations are defined in the following tables:

Table 2: SDRAM Non Mixed-Mode Module Configurations

Config #	SO-DIMM Capacity	SO-DIMM Organization	SDRAM density	SDRAM Organization	# of SDRAMs	# Rows of SDRAM	# Banks in SDRAM	# Address bits row/bank/col
1	8 MB	1M X 64	16 Mbit	1MX16	4	1	2	11/1/8
2	16 MB	2M X 64	16 Mbit	1MX16	8	2	2	11/1/8
3	32 MB	4M X 64	64 Mbit	4MX16	4	1	4	12/2/8
4	64 MB	8M X 64	64 Mbit	4MX16	8	2	4	12/2/8
5	64 MB	8M X 64	128 Mbit	8MX16	4	1	4	12/2/9
6	128 MB	16M X 64	128 Mbit	8MX16	8	2	4	12/2/9
7	128 MB	16M X 64	256 Mbit	16MX16	4	1	4	13/2/9
8	256 MB	32M X 64	256 Mbit	16MX16	8	2	4	13/2/9

Table 3: SDRAM Mixed-Mode Module Configurations

Config #	SO-DIMM Capacity	SO-DIMM Organization	SDRAM density	SDRAM Organization	# of SDRAMs	# of Rows of SDRAM	Banks in SDRAM	# Address bits row/bank/col
M1	40 MB	1M x 64 + 4M x 64	16 Mb 64 Mb	1Mb x16 4Mb x 16	4 4	2	2 4	11/1/8 12/2/8
M2	72 MB	1M x 64 + 8M x 64	16 Mb 128 Mb	1Mb x 16 8Mb x 16	4 4	2	2 4	11/1/8 12/2/9
M3	136 MB	1M x 64 + 16M x 64	16 Mb 256 Mb	1Mb x 16 16Mb x 16	4 4	2	2 4	11/1/8 13/2/9
M4	96 MB	4M x 64 + 8M x 64	64 Mb 128 Mb	4Mb x 16 8Mb x 16	4 4	2	4 4	12/2/8 12/2/9
M5	160 MB	4M x 64 + 16M x 64	64 Mb 256 Mb	4Mb x 16 16Mb x 16	4 4	2	4 4	12/2/8 13/2/9
M6	192 MB	8M x 64 + 16M x 64	128 Mb 256 Mb	8Mb x 16 16Mb x 16	4 4	2	4 4	12/2/9 13/2/9

The following SO-DIMMS will be designed at Intel and offered as reference designs.

Table 4: SO-DIMM Reference Designs

Config #	SO-DIMM Capacity	SDRAM density	SDRAM Organization	# Rows of SDRAM	# Banks in SDRAM	Size of SO-DIMM	Corresponding Figure
3 / 5 / 7	32 MB / 64 MB / 128 MB	64, 128, 256 Mbit	4MX16 / 8MX16 / 16MX16	1	4	1.00	Figure 2
4 / 6 / 8	64 MB / 128 MB / 256 MB	64, 128, 256 Mbit	4MX16 / 8MX16 / 16MX16	2	4	1.25	Figure 1

Distinction between "banks" and "rows"

This document only uses "banks" when referring to banks of memory internal to the SDRAM component (two or four). "Rows" is used to define the number of sets of SDRAMs on the SO-DIMM that collectively make up 64 bits of data.

2.0 Environmental Requirements

The SDRAM SO-DIMM shall be designed to operate within a notebook personal computer in a variety of environments. The temperature and humidity limits are as follows.

Table 5: SO-DIMM Environmental Requirements

Operating Temperature	0 °C to +65 °C ambient
Operating Humidity	10% to 90% relative humidity, noncondensing
Operating Pressure	10.106 PSI (up to 10,000 ft.)
Storage Temperature	-40 °C to + 70 °C
Storage Humidity	5% to 95% without condensation
Storage Pressure	1.682 PSI (up to 50,000 ft.) at 50 °C

Safety - UL Rating

Printed circuit board to have a flammability rating of 94V-O Markings to include UL tractability requirements per *UL Recognized Component Directory.*

3.0 Mechanical Design

The following table and drawings give the specific dimensions and tolerances for a 144-pin SO-DIMM.

Table 6: SO-DIMM Dimensions and Tolerances

SYMBOL	DEFINITION	MIN	NOM	MAX	NOTES
A	Overall module height measured from Datum -B-.	25.25 mm	25.40 mm	25.55 mm	Two sizes available: "1 inch" and "1.25 inch".
		31.60 mm	31.75 mm	31.90 mm	
A1	The distance from Datum -B- to the centerline of the PWB alignment holes	6.00 mm BASIC			These holes are not used by the next level of assembly. The dimensions are supplied for information only. If the holes are used in manufacturing they should be tightly toleranced. The recommended positional tolerance is 0.10 mm.
A2	The distance from Datum -B- to the lower edge of the Component Area on the front side of the PWB.	3.2 mm			
A3	The distance from Datum -B- to the lower edge of the Component Area on the back side of the PWB.	4.0 mm			Dimensions applicable when components mounted on both sides. Application note: border of component area.
A4	The distance from Datum -B- to the centerline of the latch holes	20.00 mm BASIC			
D	The overall length of the PWB	67.45 mm	67.60 mm	67.75 mm	
D1	The distance between the centerline of the contact at the immediate left of the key zone and the inner edge of the left latch hole.	24.50 mm BASIC			
D2	The distance between the inner edge of the latch holes	63.60 mm BASIC			
D3	The distance between Datum -A- and the center of the contact at the immediate left of the key zone on the front side of the PWB.	2.50 mm BASIC			The position of the notch indicates that the operating voltage is 3.3 Volts. The centerlines of contacts on the front side of the PWB are not coincident with the centerlines of contacts on the backside of the PWB
D4	The distance between Datum -A- and the center of the contact at the immediate left of the key zone on the backside of the PWB.	2.10 mm BASIC			
D5	The distance between the centerline of D Datum -A-.	4.80 mm BASIC			
E	The overall thickness of the PWB with the components mounted. The overall thickness is measured from the highest component on the front side to the highest component on the backside			3.80 mm	Dimensions applicable when components mounted on both sides.
e1	The distance between the centerline of the contact to the immediate left of the key zone and the center of the left most contact.	23.20 mm BASIC			
e2	The distance between the centerline of the contact to the immediate right of the key zone and the center of the right most contact.	32.80 mm BASIC			

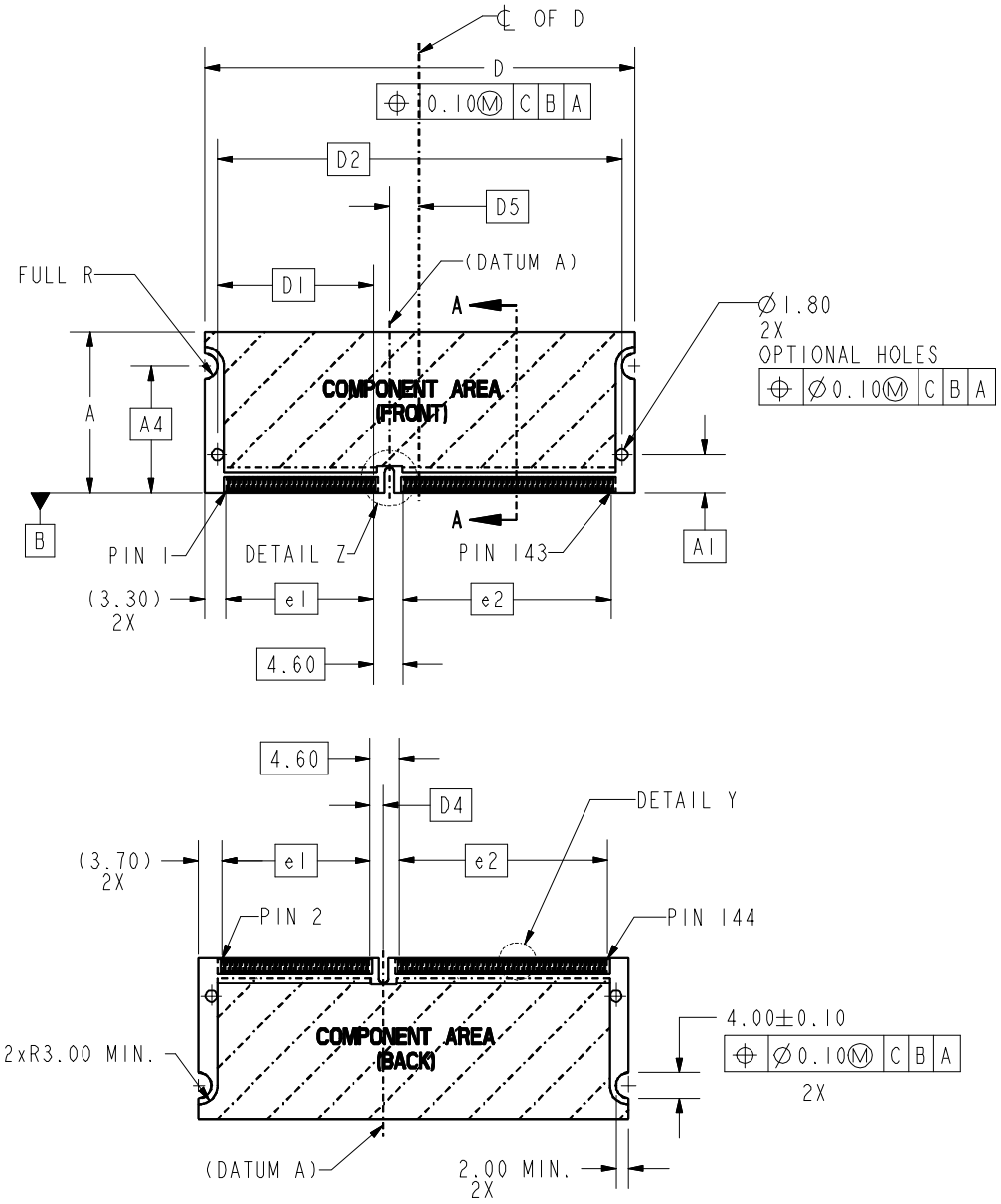


Figure 3: SO-DIMM Mechanical Drawing (1 of 5)

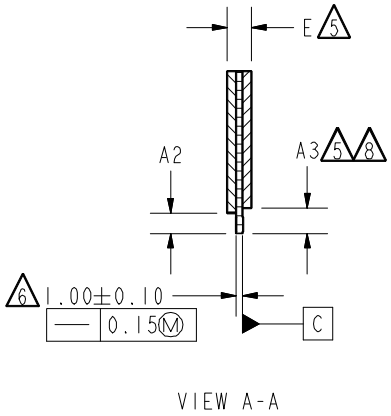


Figure 4: SO-DIMM Mechanical Drawing (2 of 5)

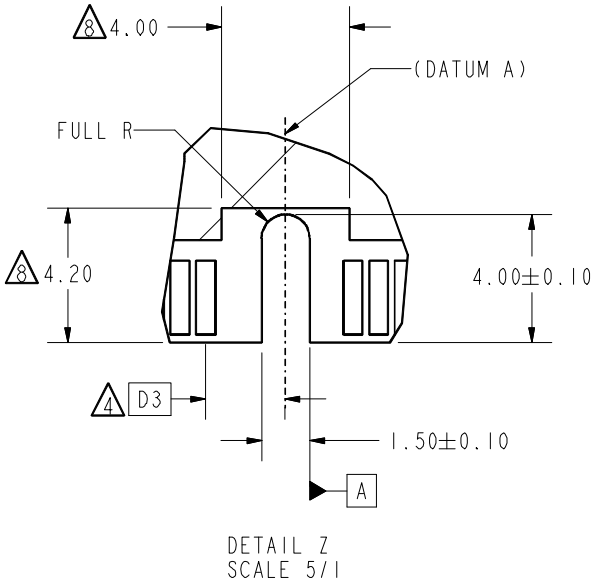


Figure 5: SO-DIMM Mechanical Drawing (3 of 5)

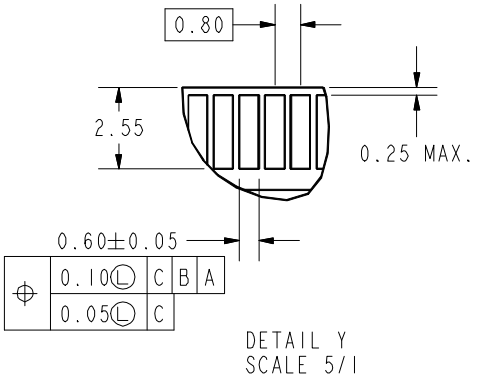


Figure 6: SO-DIMM Mechanical Drawing (4 of 5)

NOTES

1 DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.

2 TOLERANCES ON ALL DIMENSIONS +/- 0.15 UNLESS OTHERWISE SPECIFIED.

3 ALL DIMENSIONS ARE IN MILIMETERS.

4 APPLICATION NOTE:
VARYING THE POSITION OF THE NOTCH IDENTIFIES THE OPERATIONAL VOLTAGE. THE SO-DIMMS GENERATED FROM THIS SPECIFICATION OPERATE USING A VDDQ VOLTAGE OF 3.3 VOLTS.

5 DIMENSION APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH SIDES

6 CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

7 APPLICATION NOTE:
RECOMMENDED PLATING FOR CONTACT PADS SHALL BE ELECTROLYTIC GOLD PLATING 0.78 MICROMETER MIN. OVER NICKEL PLATING 2 MICROMETER MIN.

8 APPLICATION NOTE:
BORDER OF COMPONENT AREA.

Figure 7: SO-DIMM Mechanical Drawing (5 of 5)

Explanation of SO-DIMM Keying

All SO-DIMMs generated from this spec should have a notch cut into the edge connection that conveys information on the voltage of the SO-DIMM. The notch should be positioned between SO-DIMM pins 59 and 61 and should be centered between the two pins. This signifies that the SO-DIMM operates using a Vddq voltage of 3.3 Volts. Please see the mechanical drawings above for exact dimensions and placement of the notch.

4.0 Module Pinout

The following table provides the 144-pin, 64-bit unbuffered SO-DIMM module connector pinout. Note that all odd-numbered pads reside on the primary (front) side of the SO-DIMM card, and all even-numbered pins reside on the secondary (back) side of the card.

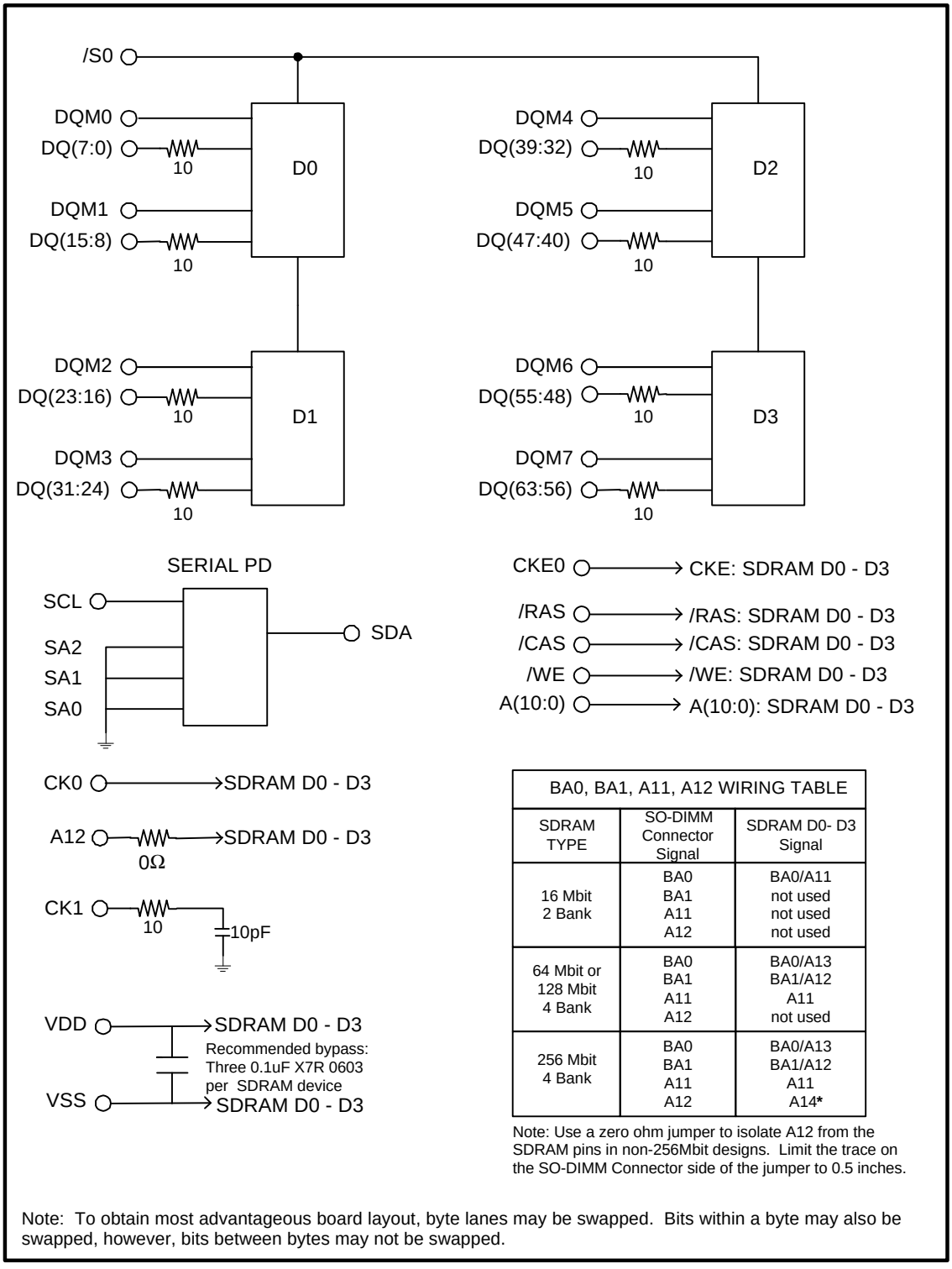
Table 7: SDRAM SO-DIMM pinout

Signal Name	Pin	Pin	Signal Name
Vss	1	2	Vss
DQ0	3	4	DQ32
DQ1	5	6	DQ33
DQ2	7	8	DQ34
DQ3	9	10	DQ35
Vdd	11	12	Vdd
DQ4	13	14	DQ36
DQ5	15	16	DQ37
DQ6	17	18	DQ38
DQ7	19	20	DQ39
Vss	21	22	Vss
DQMB0	23	24	DQMB4
DQMB1	25	26	DQMB5
Vdd	27	28	Vdd
A0	29	30	A3
A1	31	32	A4
A2	33	34	A5
Vss	35	36	Vss
DQ8	37	38	DQ40
DQ9	39	40	DQ41
DQ10	41	42	DQ42
DQ11	43	44	DQ43
Vdd	45	46	Vdd
DQ12	47	48	DQ44
DQ13	49	50	DQ45
DQ14	51	52	DQ46
DQ15	53	54	DQ47
Vss	55	56	Vss
Reserved	57	58	Reserved
Reserved	59	60	Reserved
CLK0	61	62	CKE0
Vdd	63	64	Vdd
RAS#	65	66	CAS#
WE#	67	68	CKE1
S0#	69	70	A12

Signal Name	Pin	Pin	Signal Name
S1#	71	72	A13
Reserved	73	74	CLK1
Vss	75	76	Vss
Reserved	77	78	Reserved
Reserved	79	80	Reserved
Vdd	81	82	Vdd
DQ16	83	84	DQ48
DQ17	85	86	DQ49
DQ18	87	88	DQ50
DQ19	89	90	DQ51
Vss	91	92	Vss
DQ20	93	94	DQ52
DQ21	95	96	DQ53
DQ22	97	98	DQ54
DQ23	99	100	DQ55
Vdd	101	102	Vdd
A6	103	104	A7
A8	105	106	BA0
Vss	107	108	Vss
A9	109	110	BA1
A10	111	112	A11
Vdd	113	114	Vdd
DQMB2	115	116	DQMB6
DQMB3	117	118	DQMB7
Vss	119	120	Vss
DQ24	121	122	DQ56
DQ25	123	124	DQ57
DQ26	125	126	DQ58
DQ27	127	128	DQ59
Vdd	129	130	Vdd
DQ28	131	132	DQ60
DQ29	133	134	DQ61
DQ30	135	136	DQ62
DQ31	137	138	DQ63
Vss	139	140	Vss
SDA	141	142	SCL
Vdd	143	144	Vdd

Note: Reserved = Do not connect

5.0 SDRAM SO-DIMM Block Diagrams

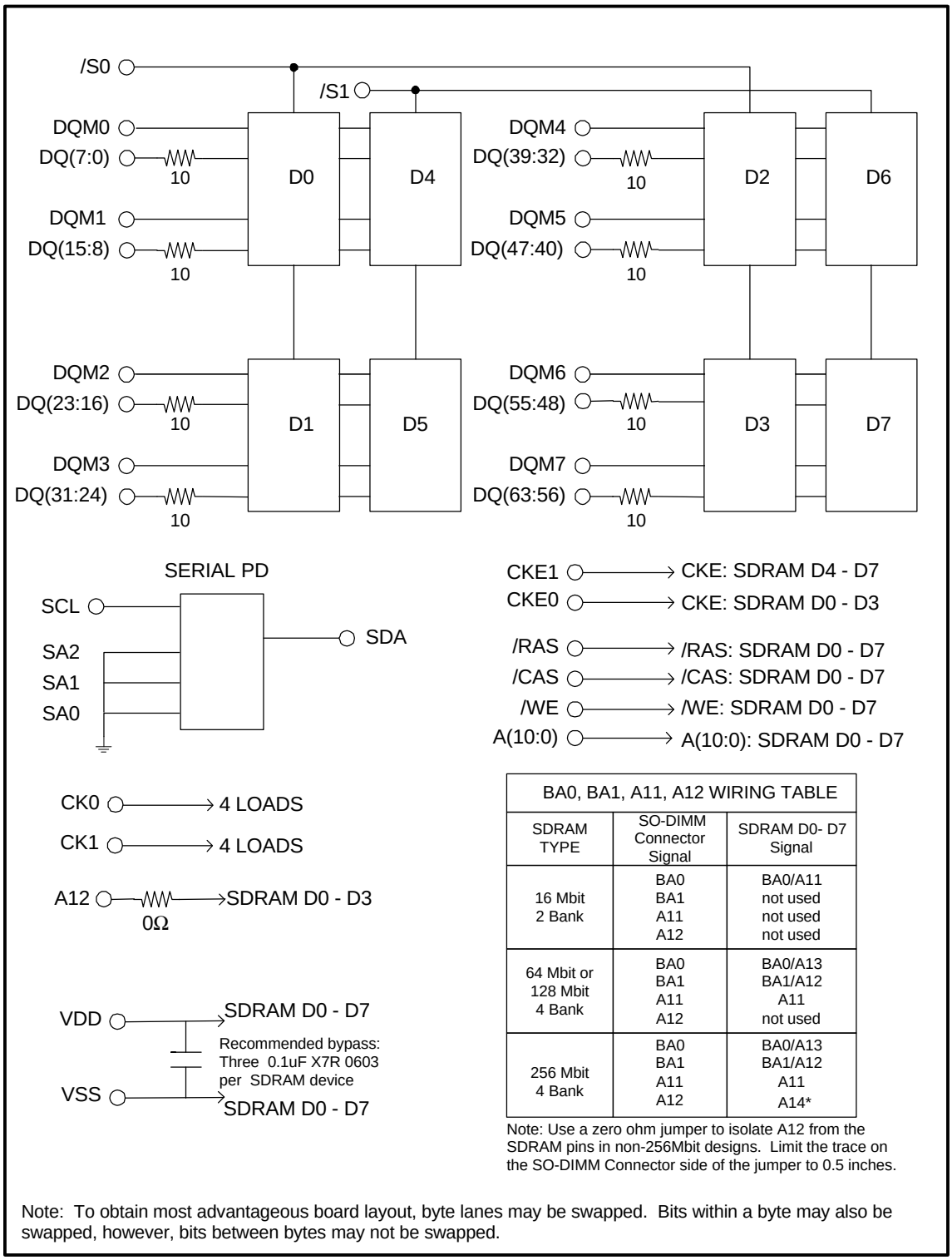


BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	SO-DIMM Connector Signal	SDRAM D0- D3 Signal
16 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit or 128 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used
256 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 A14*

Note: Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs. Limit the trace on the SO-DIMM Connector side of the jumper to 0.5 inches.

Note: To obtain most advantageous board layout, byte lanes may be swapped. Bits within a byte may also be swapped, however, bits between bytes may not be swapped.

Figure 8: 64-bit non-ECC SO-DIMM Block Diagram (1 Row, x16 SDRAMs)



BA0, BA1, A11, A12 WIRING TABLE		
SDRAM TYPE	SO-DIMM Connector Signal	SDRAM D0- D7 Signal
16 Mbit 2 Bank	BA0 BA1 A11 A12	BA0/A11 not used not used not used
64 Mbit or 128 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 not used
256 Mbit 4 Bank	BA0 BA1 A11 A12	BA0/A13 BA1/A12 A11 A14*

Note: Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs. Limit the trace on the SO-DIMM Connector side of the jumper to 0.5 inches.

Note: To obtain most advantageous board layout, byte lanes may be swapped. Bits within a byte may also be swapped, however, bits between bytes may not be swapped.

Figure 9: 64-bit non-ECC SO-DIMM Block Diagram (2 Rows, x16 SDRAMs)

6.0 SO-DIMM PCB Layout and Signal Routing

Printed Circuit Board

The SO-DIMM printed circuit board shall be at least a six layer stack-up using glass epoxy material. The PCB must have both a full ground plane layer and a full power plane layer. The required signal trace impedance is 55Ω ±15%. Components shall be of surface mount type, and may be mounted on one or both sides of the PCB.

Table 8: PCB Calculated Parameters

Parameter	Min	Max
Propagation delay: S_0 [ps/in] (outer layers)	141	153
Propagation delay: S_0 [ps/in] (inner layers)	167	180
Trace impedance: Z_0 [Ω] (all layers)	47	63

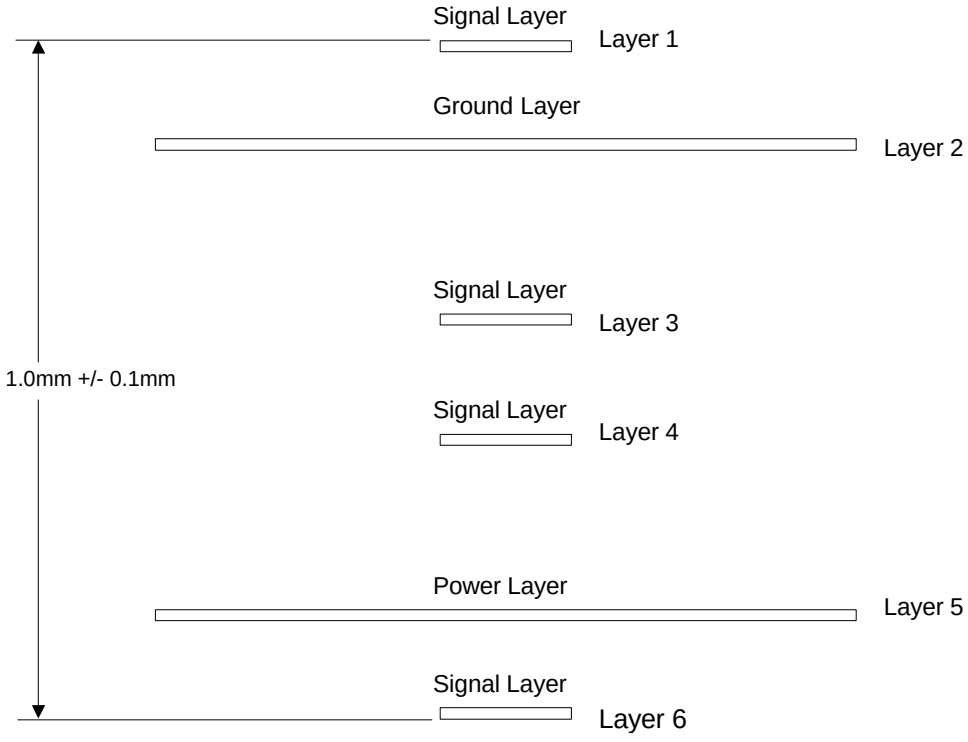


Figure 10: Example 6-layer PCB Stackup

Edge Connection

The PCB edge connector contacts shall be gold plated per Figure 7, Note 7. Note: The PCB connector edge will not be chamfered.

EMI Reduction

To minimize radiation from clock traces on the SO-DIMMs, the following are requirements:

- Clocks must be routed with as much of the trace on an inner signal layer as possible.
- Clocks on the inner layer will have a 5 mill ground trace surrounding them, with vias stitched to ground at 0.5" intervals, or as often as routing allows.
- Both internal signal layers and the power plane should have a ground ring routed around the perimeter of the board and stitched to ground at intervals <0.5". The ground rings should be on the order of 20 mils wide, but can be reduced to 10 mils in areas where 20 mils cannot be accommodated.

Component Types and Placement

Components shall be of surface mount type, and may be mounted on one or both sides of the PCB. Components shall be positioned on the PCB to meet the min and max trace lengths required for SDRAM data signals. Bypass capacitors for SDRAM devices must be located as near as practical to the device power pins. It is also important to place each SDRAM in the optimum position to ensure meeting of trace length and topology requirements. Pin swapping of data pins within individual bytes should also be used for the same reason.

Exact spacing numbers are not provided, but are left up to the SO-DIMM manufacturer to determine based on manufacturing constraints and signal routing constraints imposed by this specification.

Signal Groups

In this specification, the SDRAM timing-critical signals have been divided into groups whose members have identical loading and routing topologies. The following table summarizes the signal groups by listing the signals contained in each. The following sections will describe routing restrictions associated with each signal group.

Table 9: Signal Topology Categories

SIGNAL GROUP	SIGNALS IN GROUP
Clock	CLK [1:0]
Data	DQ [63:0]
Data Mask	DQMB [7:0]
Chip Select	S#[1:0]
Clock Enable	CKE[1:0]
Double cycle signals	A[12:0]
	BA[1:0]
	RAS#
	CAS#
	WE#

Signal Topology and Length Restrictions

In order to meet signal quality and setup/hold time requirements for the memory interface, certain routing topologies and trace length requirements must be met. The signal topology requirements are shown pictorially in the following pages. Each topology diagram is accompanied by a trace length table that lists the minimum and maximum lengths allowed for each trace segment and, where applicable, the min and max lengths for the entire net. Each diagram also shows where vias are allowed or includes a note that specifies where vias are allowed if they are not shown in the diagram.

Routing Rules

General Info: All signal traces except clocks are routed using 5/5 rules.
(5 mil traces and 5 mil minimum spacing between adjacent traces).

Clocks are routed using 5 mil traces and 5 mil space to the 5 mil ground trace.

No test points are required.

Topology Diagram Explanation

The routing topology diagrams in this section are intended to be used to determine individual signal topologies on a SO-DIMM for any supported configuration.

These diagrams are read as follows:

Only the cylinders labeled with length designators represent actual physical trace segments. All other lines should be considered zero in length.

All loads and traces outside of the dashed boxes constitute the base topology which covers the minimum loading case for each signal.

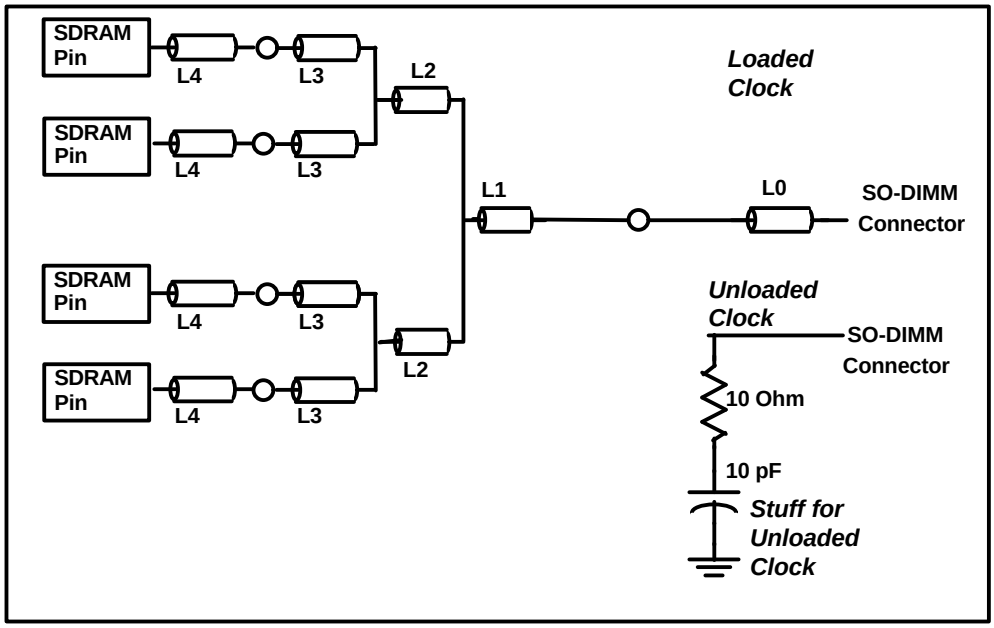
Allowed vias are either shown as circles on the topology diagrams or are otherwise documented under each diagram in a separate note.

The topology for a given configuration can be determined by adding the traces and loads within the dashed boxes to the base topology. Add only the traces and loads within boxes that apply for the desired configuration.

The permitted segment length ranges for that topology are read from the table below each topology diagram.

Topology for Clock: CLK[1:0]

Special attention must be given to the routing of the SDRAM clock signal(s) to ensure adequate signal quality, rise/fall time, minimum skew between clock edges at each SDRAM component, and predictable skew to motherboard chipset clocks. For that reason, all utilized clocks are made to look electrically similar by loading them with exactly four SDRAM loads. Clock signals must have either four SDRAM loads, or they must be terminated into 10 ohms and 10 pF. Trace lengths to the RC termination of unloaded clocks must be kept to an absolute minimum. Clock traces must be 5 mils wide with 15 mil spacing to any other signal including the clocks themselves.



Note: Either the L2 or the L3 trace segment may contain one additional via which is not shown in the diagram.

Figure 11: Signal routing topologies for Clocks

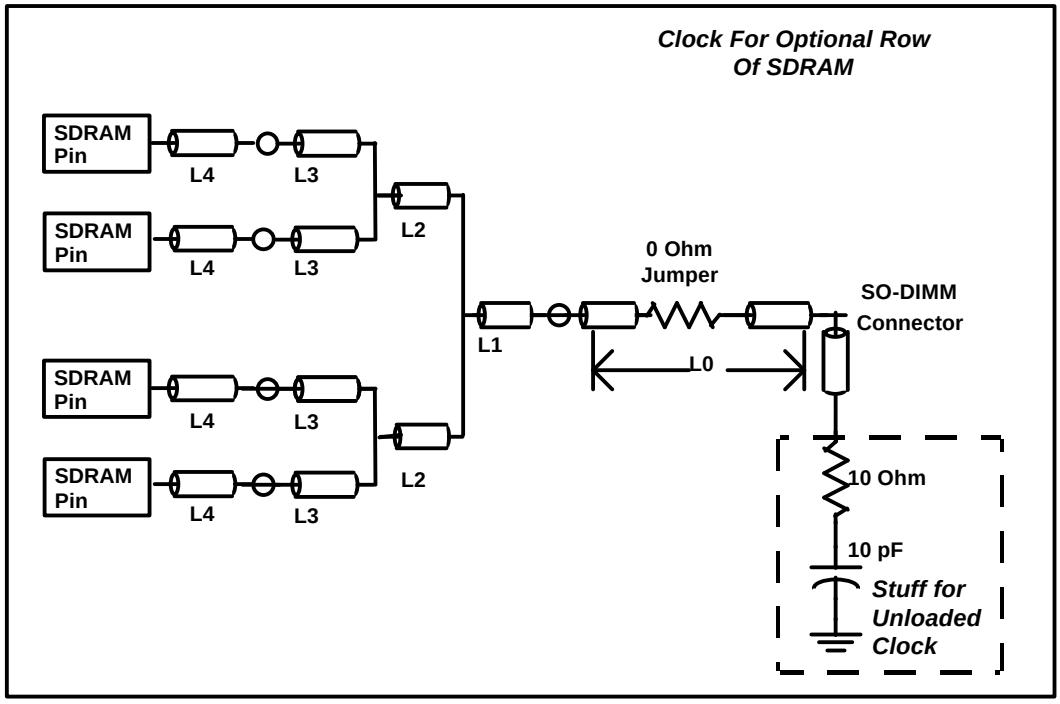
Table 10: Trace Length Table for Clock Topologies

Segment	L0	L1	L2	L3	L4	Total Min	Total Max
Length	0.10	1.00	0.80	0.50	0.10	2.45	2.55
Tolerance	± 0.05	± 0.02	± 0.02	± 0.02	± 0.05		
Layer	Outer	Inner	Inner	Inner	Outer		

1 All distances are given in inches and should be kept within tolerance, and routed on the indicated layer.
2 Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2 + L3 + L4. Also, the total min and max limits are tighter than the sum of the individual min and max lengths. This implies that not all individual segment lengths may be adjusted to the min or max value at the same time.

Topology for Clock with an option to not stuff a row of SDRAM: CLK[1]

If the PB is designed with the option to not stuff a row of SDRAM, a jumper must be included to disconnect the clock tree from the RC termination. The overall length of the net from the SO-DIMM pin to the SDRAM pin, through the jumper, must be the same as for clocks without this option. The diagram and table below explain this. In the picture, L0 is the sum of the trace lengths on both sides of the 0Ω jumper, and the distance through the 0Ω jumper. Trace lengths to the RC termination must be kept to an absolute minimum.



Note: Either the L2 or the L3 trace segment may contain one additional via which is not shown in the diagram.

Figure 12: Signal routing topologies for Clocks to Rows with Optional Stuffing

Table 11: Trace Length Table for Clocks to Rows with Optional Stuffing

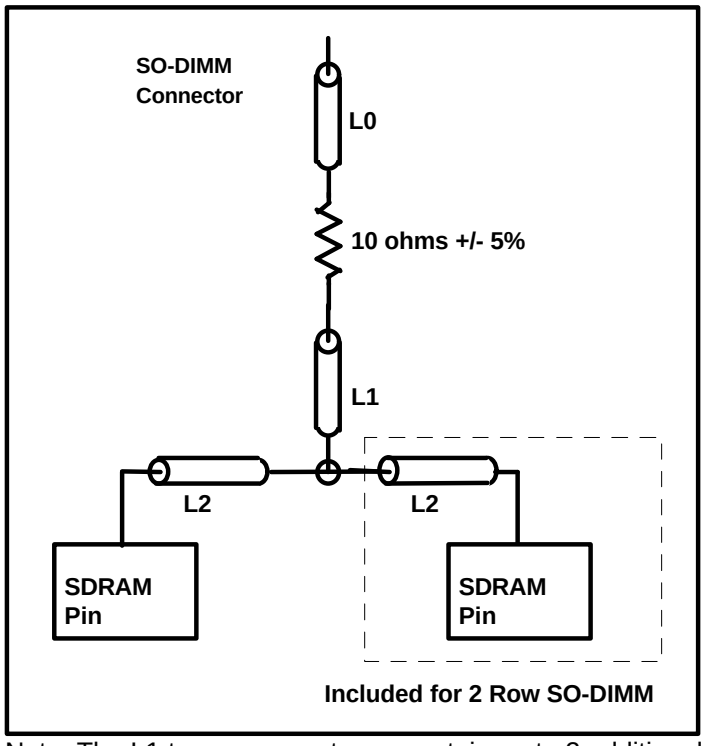
Segment	L0	L1	L2	L3	L4	Total Min	Total Max
Length	0.25	0.85	0.80	0.50	0.10	2.45	2.55
Tolerance	± 0.05	± 0.02	± 0.02	± 0.02	± 0.05		
Layer	Outer	Inner	Inner	Inner	Outer		

1 All distances are given in inches and should be kept within tolerance, and routed on the indicated layer.
2 Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2 + L3 + L4. Also, the total min and max limits are tighter than the sum of the individual min and max lengths. This implies that not all individual segment lengths may be adjusted to the min or max value at the same time.

Topology for Data: DQ[63:0]

These signals are routed using a balanced "T" topology on any layer. The table defines the line length ranges allowed for these signals.

Figure 13: Signal routing topologies for Data



Note: The L1 trace segment may contain up to 2 additional vias which are not shown in the diagram.

Table 12: Trace Length Table for Data Topologies

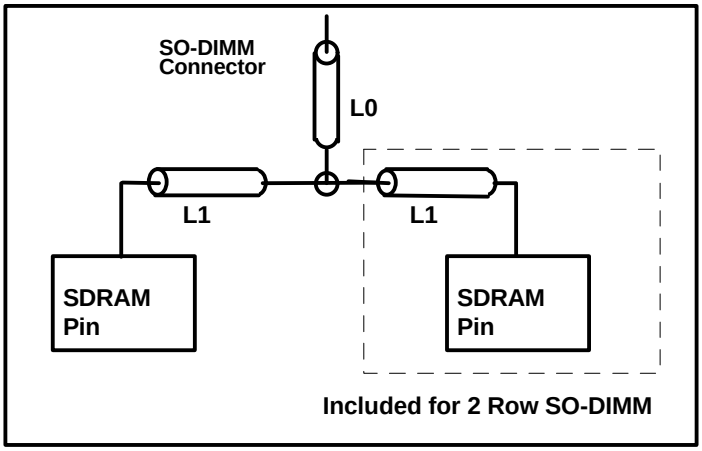
Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	Total Min	Total Max
X16	1/2	0.10	0.50	0	0.90	0	0.25	0.60	1.00

1 All distances are given in inches

2 Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2. Also, the total min and max limits are tighter than the sum of the individual min and max lengths. This implies that not all individual segment lengths may be adjusted to the min or max value at the same time.

Topology for Data Mask: DQMB[7:0]

These signals are routed using a balanced "T" topology on any layer. The tables define the line length ranges allowed for these signals.



Note: The L0 trace segment may contain 1 additional via which is not shown in the diagram.

Figure 14: Signal routing topologies for Data Mask (1/2 Loads)

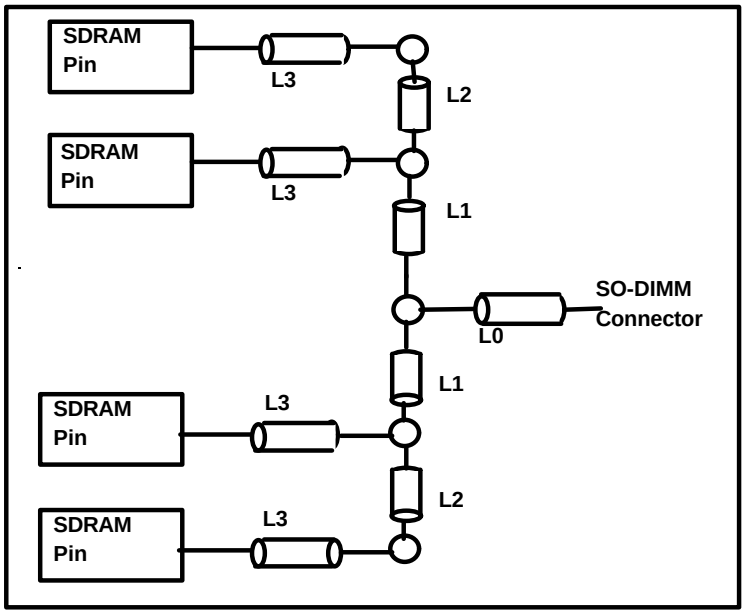
Table 13: Trace Length Table for Data Mask Topologies (1/2 Loads)

Comp Width	# loads	L0 Min	L0 Max	L1 Min	L1 Max	Total Min	Total Max
X16	1/2	0.75	1.10	0.00	0.30	1.00	1.40

1 All distances are given in inches

Topology for Chip Select: S#[1:0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for these signals.



Note: The L0 trace may contain up to 2 vias which are not shown in the diagram.

Figure 15: Signal routing topologies for Chip Select

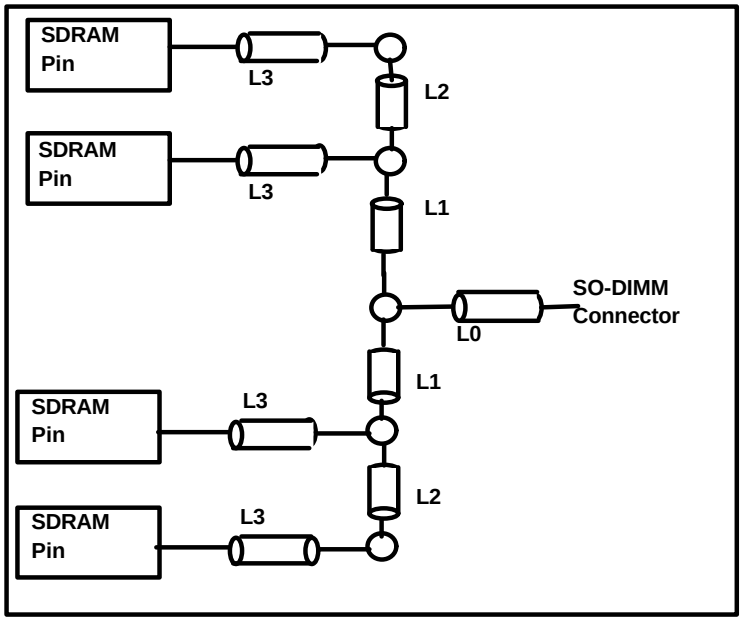
Table 14: Trace Length Table for Chip Select Topologies

Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	Total Min	Total Max
x16	4	0.50	1.10	0.10	0.50	0.0	0.60	0.05	0.35	1.00	2.30

1 All distances are given in inches.
2 Total distance is L0+L1+L3 or L0+L1+L2+L3. SO-DIMM connector to SDRAM Pin.

Topology for Clock Enable: CKE#[1:0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for each trace segment.



Note: The L0 trace may contain up to 2 vias which are not shown in the diagram.

Figure 16: Signal routing topologies for Clock Enable

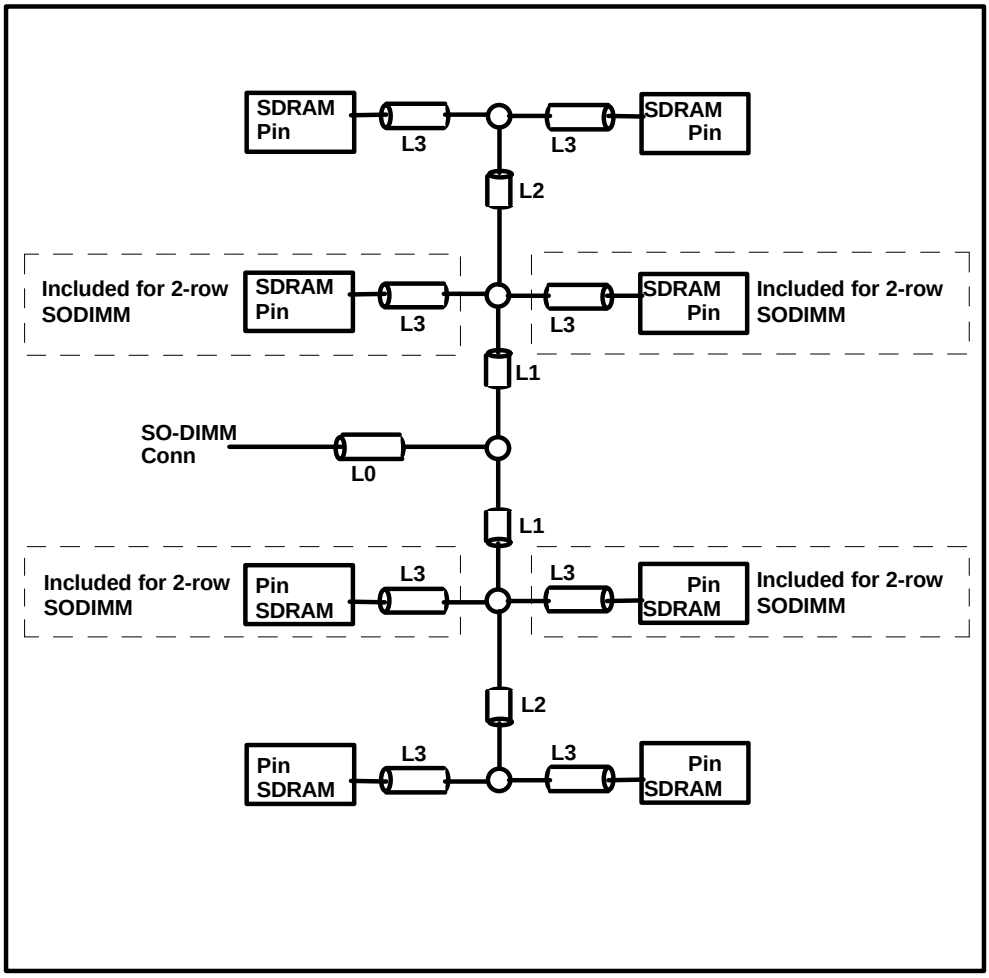
Table 15: Trace Length Tables for Clock Enable Topologies

Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	Total Min	Total Max
x16	4	0.50	1.10	0.0	0.50	0.0	1.00	0.05	0.35	1.0	2.3

1 All distances are given in inches.
2 Total distance is L0+L1+L3 or L0+L1+L2+L3. SO-DIMM connector to SDRAM Pin.

Double Cycle Signals: MAx, BAx, SRAS#, SCAS#, WE#

These signals are routed using a balanced, double-sided "comb" topology on any layer. The table below defines the line length ranges allowed for these signals.



Note: The L0 trace may contain up to 2 vias which are not shown in the diagram.

Figure 17: Signal routing topologies for Double Cycle Signals

Table 16: Trace Length Table for Double Cycle Signal Topologies

Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	Total Min	Total Max
x16	4/8	0.50	2.50	0.0	1.10	0.0	1.00	0.10	0.40	0.75	4.0

1 All distances are given in inches
2 Total distance is L0+L1+L3 or L0+L1+L2+L3. SO-DIMM connector to SDRAM Pin.

7.0 SO-DIMM PCB and Final Assembly Labeling Requirements

Printed Circuit Board Labeling

The printed circuit board is required to have the following labeling contained in etch or silk-screen:

Vendor name and part number
Flammability indicator (see Section 2 of this document, under Safety)
The text: SO-DIMM-REV#.#
(#.# corresponds to the revision of this SO-DIMM spec to which the PCB is designed)

Assembled SO-DIMM Naming Convention

In order to be able to visually identify the critical parameters of a given SO-DIMM, the following naming convention will be used.

On component or sticker on DIMM (supplier option):
- use minimum 8point font

PCX-abc-def
Where X=MHz
a = CL value
b = trcd value
c = trp value
d = tac value
e = spd rev #
f = reserved

Example: PC100-322-620
is 100MHz, CL3, trcd=2, trp=2, tac=6, 2= spd rev 1.2 with the last digit reserved.

Note: A two digit designator for both the tac and spd fields is optional if appropriate.

Example: PC100-322-06120
is also 100MHz, CL3, trcd=2, trp=2, tac=6, 12= spd rev 1.2 with the last digit reserved.

8.0 SDRAM Component Specifications

The SDRAM components used with this 66/100 MHz SO-DIMM design spec MUST adhere to the most recent revision of the Intel “PC SDRAM Specification." Please refer to that document for all technical specifications and requirements of the SDRAM devices. Any violation of the requirements of the Intel PC SDRAM Component Specification constitutes a violation of the 66/100 MHz PC SDRAM Unbuffered SO-DIMM Specification.

9.0 EEPROM Component Specifications

The Serial Presence Detect function MUST be implemented on the PC SDRAM SO-DIMM. The component used and the data contents must adhere to the most recent version of the Intel "SDRAM Serial Presence Detect Specification". At the time of this writing, the current revision is 1.2A. Please refer to that document for all technical specifications and requirements of the serial presence detect devices. Any violation of the requirements of the Intel SDRAM Serial Presence Detect specification constitutes a violation of the PC SDRAM Unbuffered SO-DIMM Specification.